Design of CMOS Serializer

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Abstract – **SoCs technologies are growing at a faster rate therefore it demand integration of large amount of buses and metal tracks for interconnections .ASerializer/Deserializer (SerDes) is a device that receipts the parallel data link input andcondenses it into fewer lines of serial stream which would then deserialized and output as theoriginal recovered parallel data. SerDes is more beneficial because it solves the issues like data skew , cross talk. This paper presents a description on design of a various Serializer architecture that is used to do the serialization function in On-Chip SerDes Transceiver. Phase Locked Loop is designed with a frequency of 100MHz which is used for clock generation.The proposed design is synthesized using CADENCE VIRTUOSO and the experimental evaluation using CADENCE EDA simulations with gpdk180nm CMOS standard cell technology. Power and delay are estimated in order to evaluate the performance of the proposed design.**

1. INTRODUCTION

A.High Speed SERDES

A Serializer/Deserializer (SerDes) is a device that permits data to transfer in a serial manner and vice versa and plays more important role in modern high speed applications.A basic block diagram of high speed SerDes is presented in Figure 1. Firstly the n-bit parallel data is serialized in the transmitter slice through a Serializer. An equalizer is then used to guarantee the best signal of the serialized data.On the receiver slice, the received serial data is then fed into a Clock Data Recovery (CDR) circuit.

After the recovery and equalization circuitries, the data is finally restored back to parallel data bus through a Deserializer circuit on the receiver slice. Here the Phase-locked loop (PLL) is used to provide the clock signals for the transmitter and receiver slice. The transmitter (TX) slice performs parallel-to-serial conversion through a Serializer circuit. The serialized data is then fed to a feed forward equalizer (FFE) to ensure that the receiver input is a clean waveform.Equalization is also required in receiver slice after the serialized data being transmitted through the channel.

A decision feedback equalizer (DFE) is required to pick up the bit error rate (BER). After that the serial stream is driven by the Deseriazlier to perform the serial-to-parallel conversion. The remainder of this paper describes the design of Serializer in more detail.
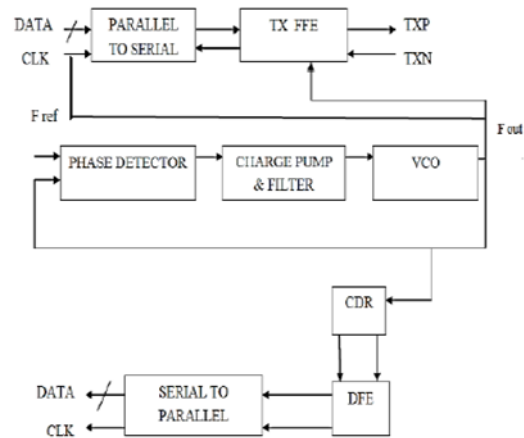

Figure 1.Overview of the Serdes Core

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2. SERIALIZER DESIGN

Serializer operation performs the parallel-to-serial conversion as shown in the below figure. A4:1 serializer is obtained from the two 2:1 serializer.In this paper we are going see about various design ofserializer in more detail. The figure shown below is the block diagram of 4:1 serializer.
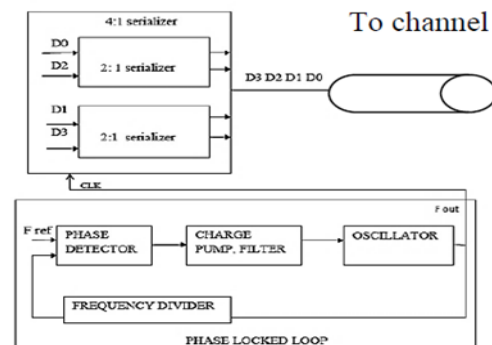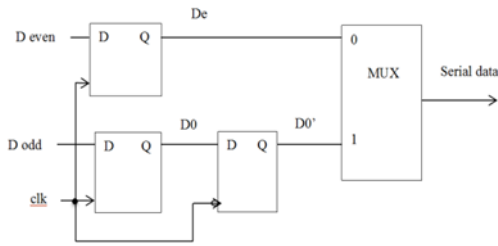

Figure 2. 4:1 serializer block

Figure 3. 2:1 Serializer block

3. D FLIP FLOP DESIGN

The D flip-flop consist of one input D input, or data input, and two outputs Q and Q'. It transfers the data at the input after the delay of one clock pulse at the output Q. So in some cases the input is referred to as a delay input and the flip-flop gets the name delay (D) flip-flop.

A.D Flip Flop NAND Logic

It can be simply constructed from an S-R flip-flop by simply incorporating an inverter between S and R such that the input of the inverter is at the S end and the output of the inverter is at the R end. The structure of the D flip-flop is being constructed using NAND gates.If the CLK is low; the value of the D input has no effect, since the S and R inputs of the basic NAND flip-flop are kept as 1.If the CLK = 1, and D = 1, the NAND gate 1 produces 0, which forces the output of NAND gate 3 as 1. On the other hand, both the inputs of NAND gate 2 are 1, which gives the output of gate 2 as 0. Hence, the output of NAND gate 4 is forced to be 1, i.e., Q = 1, whereas both the inputs of gate 5 are 1 and the output is 0, i.e., Q' = 0. Hence, we find that when D = 1, after one clock pulse passes Q = 1, which means the output follows D.If the CLK = 1, and D = 0, the NAND gate 1 produces 1. Hence both the inputs of NAND gate 3 are 1, which gives the output of gate 3 as 0. On the other hand, D = 0 forces the output of NAND gate 2 to be 1. Hence the output of NAND gate 5 is forced to be 1, i.e., Q' = 1, whereas both the inputs of gate 4 are 1 and the output is 0,i.e.,Q = 0. Hence, we find that when D = 0, after one clock pulse passes Q = 0, which means the output again follows D.
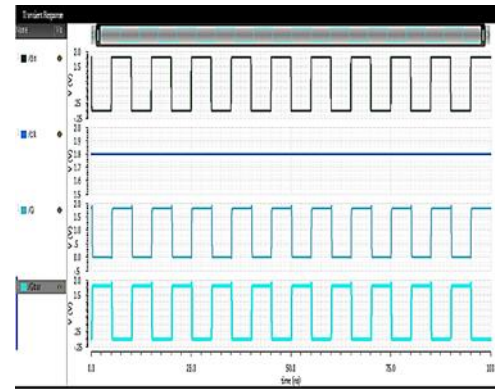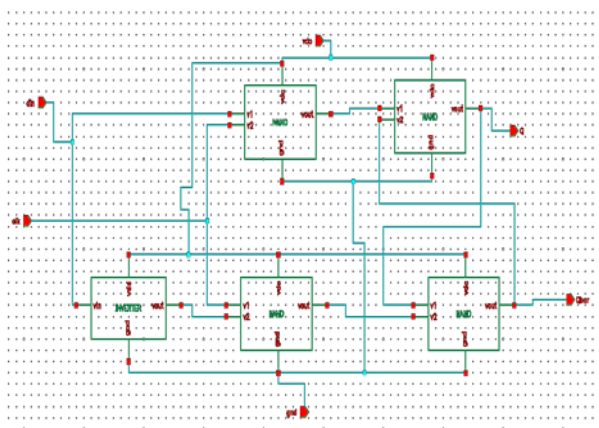

Figure 4.NAND Gate Based D FF

B.D Flip Flop Using Transmission Gates

The CMOS transmission gate consist of two MOSFETs, n-type responsible for transfer of proper zeros, and one p-type, responsible for transfer of proper logic one. When the CLK signal is high, the bottom transmission gate is on, and the flip flop is transparent – input signal D is copied to Q. During this time, the top transmission gate is off. When the CLK signal is low, the bottom transmission gate is off while the top is on. The feedback ensures the output is held as long as the CLK signal is low[10].
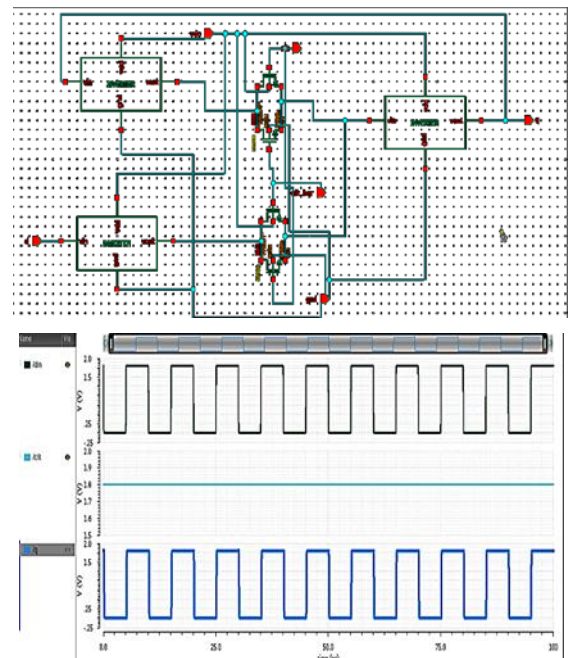

Figure5.Transmission Gate Based D FF

C.D Flip Flop Using Transistor Logic

Figure 4.6 Shows positive edge triggered 5 Transistor D flip flop[10]. If Clock and input becomes high then the transistors M1, M5 indicates off condition and remaining transistors M2,

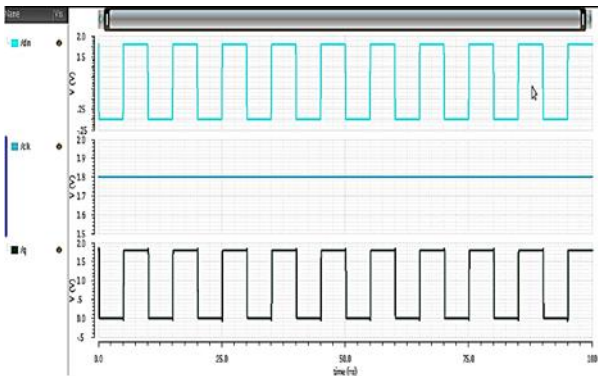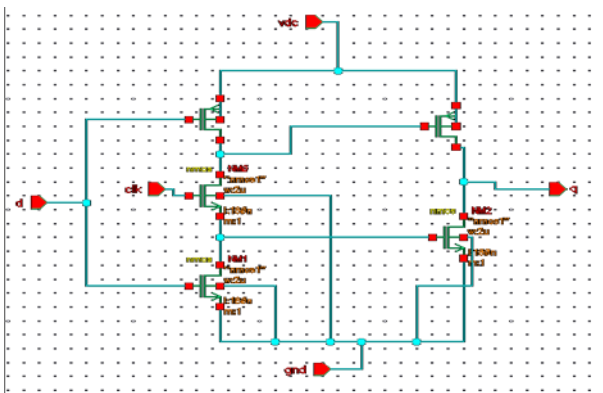M3, M4 shows on. The output becomes high.During on clock period inputdatareaches output.

Figure6.Transistor Based D FF

D.D Flip Flop Design Using Tristate Inverter

The circuit shown in Figure7, is CMOS implementation of D FF using 10 transisstor [10]. The circuit consist of two tristate inverters and driven by clock signal and transpose of it. Whenever the clock attains high, the first tri state inverter act as the input while the second tristate inverter indicates high input impedance state then the output follows the input value. While the clock attain low value , second trisate inverter finishes the two inverter loop and hold its state until the following clock signal
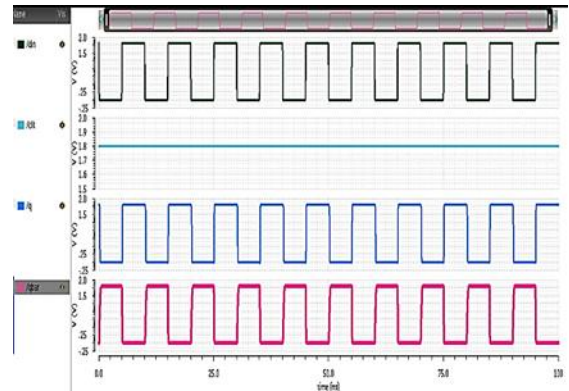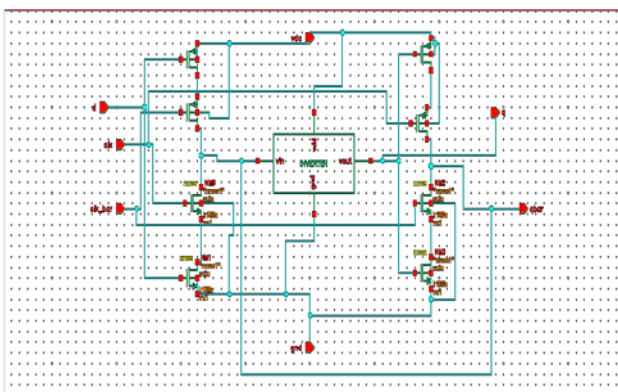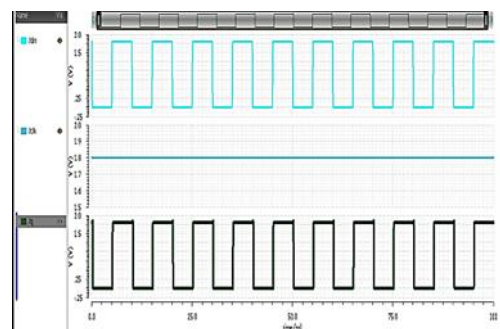

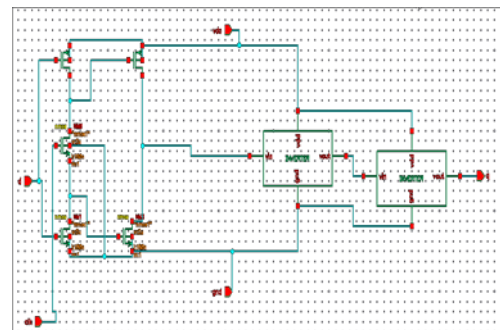

Figure7.Tristate Inverter Based D FF

E.D Flip Flop Design Using TSPC

In TSPC logic we have only clock and do not need an inverted clock. These techniques eliminate skew problems due to different clock phases. The circuit diagram of TSPC based D flip flop is shown in Figure 8.

4. MUX DESIGN

A multiplexer (or mux) is used to choose one of the analog or digital input signals and transfer the selected input into a output line.A multiplexer of 2*m*inputs has [*m*] select lines, used to select which input line need to besend to the output.

A.NAND Based MUX

The Schematic of CMOS logic based 2:1 multiplexer circuit has shown in the Figure. 9, [9] if both of the A and B inputs are high, then both the NMOS transistors will conduct, neither of

the PMOS transistors will conduct, which brings the output low. If both of the A and B inputs are low, then neither of the NMOS transistors will conduct, while both of the PMOS transistors will conduct,that brings the output high. If either of the A or B inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will,and brings the output to be high
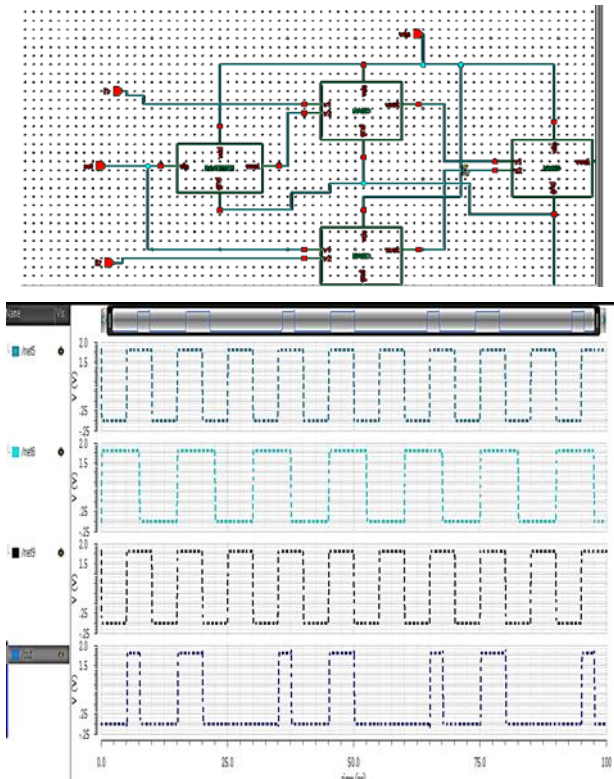

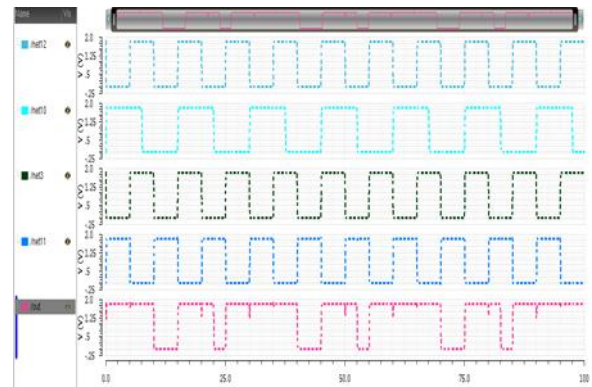Figure9.NAND Based MUX

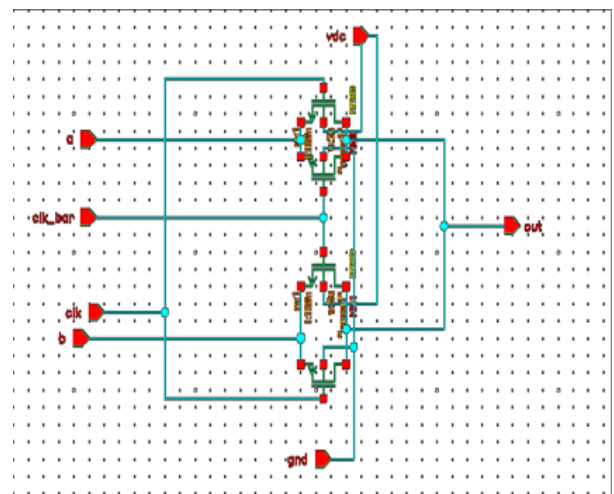*B.Transmission Gate Based MUX*

Figure10.Transmission Gate Based Mux

In this logic style N and P devices with sources and drains connected in parallel. A 2to1 multiplexer can be implemented using 6 transistors by this logic style[8].when the clock is high upper transmission gate is on and input A reaches the output an when clock is zero lower transmission gate is on ana output the value of B.
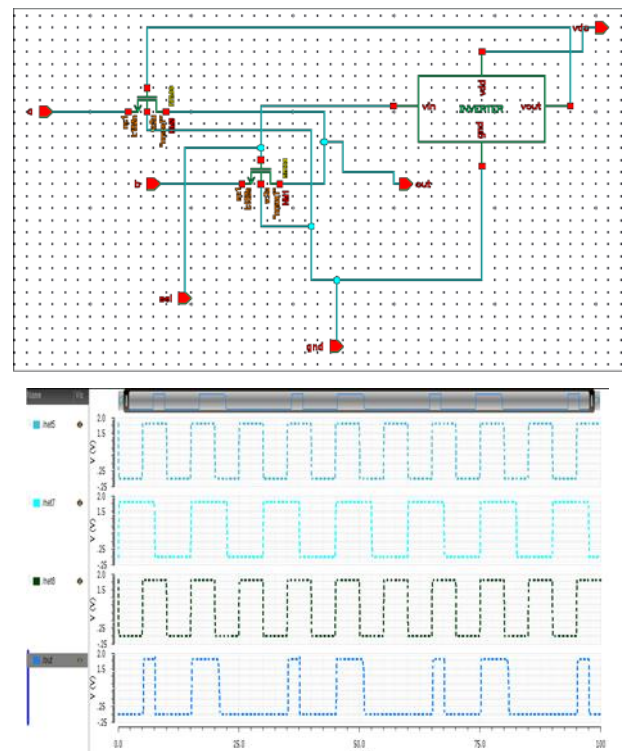
C.Pass Transistor Based MUX

Figure 11.Pass Transistor Based Mux

The pass-transistors allows the inputs to drive gate as well as source drain terminals therefore the number of transistor required to implement the logic get reduced. The advantage is that one pass-transistor network (either NMOS or PMOS) is sufficient to perform the logic operation [7]. When select signal

is low input A reaches the output and vice versa for select signal high.

D.MUX based on CMOS logic

In this design cmos logic is used which consist of both Ptype and n type transistor [8]. The signal which turns on a transistor of one type will turn off a transistor of the other type. Hence, if the gate of both transistor are connected to the same input means, the p-type MOSFET will be on when the n-type MOSFET is off, and vice-versa. A 2-to-1 multiplexer can be implemented using 12 transistors by this logic style.
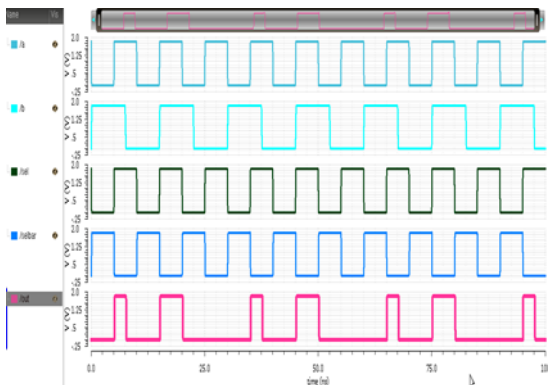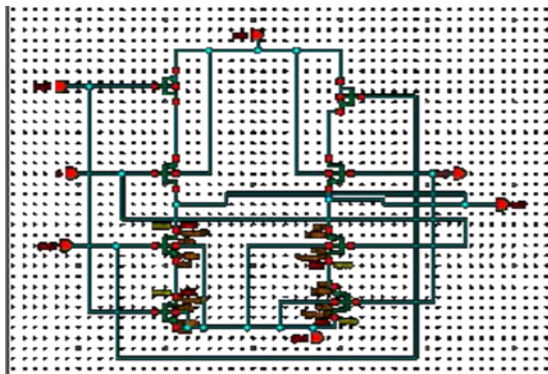

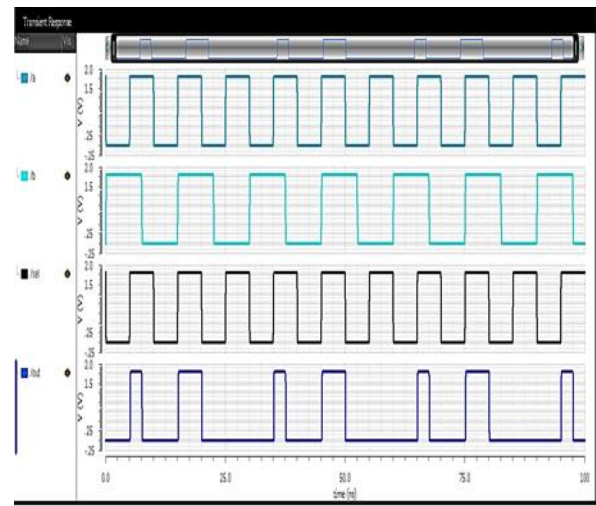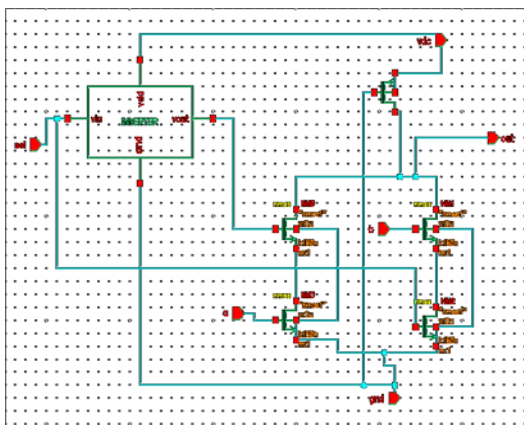Figure12.MUX based on CMOS

E.Pseudo Based MUX

Figure 13.Pseudo NMOS Based MUX

Using a single PMOS transistor as a pull-up block for an n-block is called pseudo-NMOS logic[9]. The pull-up transistor must be chosen large enough to conduct a multiple of the n-block's leakage

5. 2:1 SERIALIZER DESIGN

As we have seen in figure 2 serializer block consist of D flip flop and multiplexers and we have seen various design of D flip flop and MUX design.For designing of 4:1 serializerfirst of all we need to design 2:1 serializer. So for example here we are going to see the design of 2:1 serializer with the above mentioned D flip flop(NAND) and MUX(NAND).

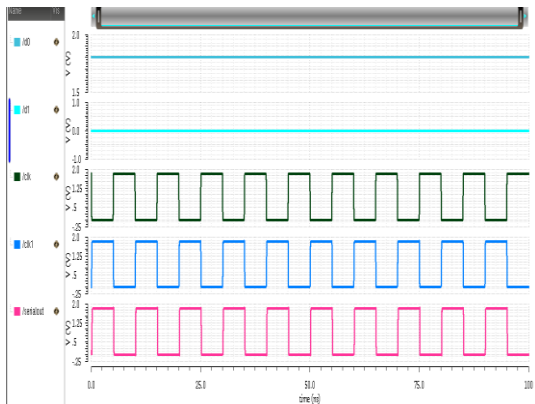A. *2:1 serializer with D flip flop (Transmission gate) and MUX (NAND)*
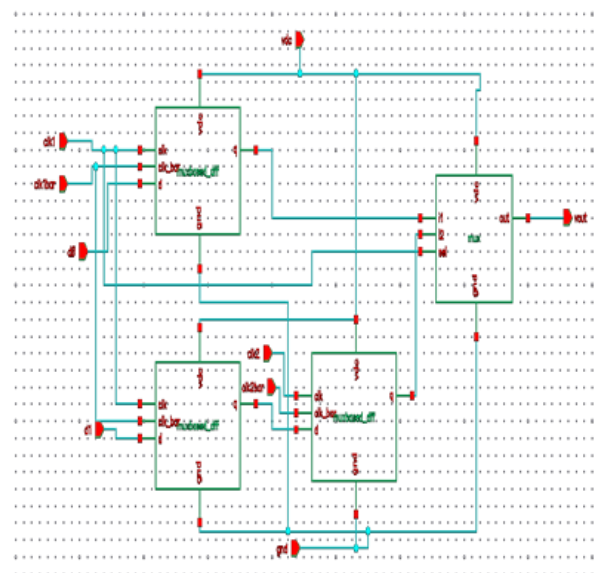
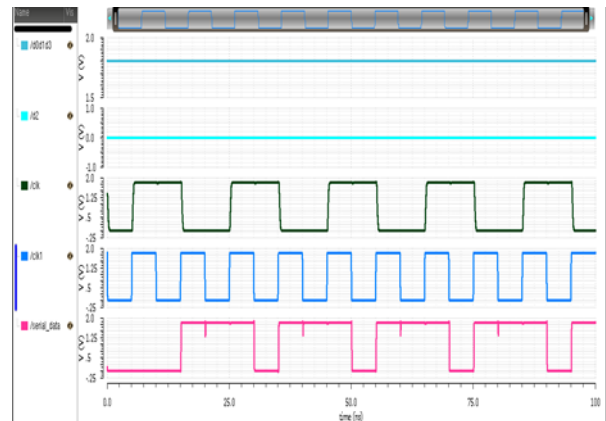Figure 14.2:1 Serializer Schematic DFF(NAND)and

MUX(NAND)

B. 4:1 Serializer

Generally 4:1 serializer is designed with the help of 2:1 serializer. Figure 15 shows the generic 4:1 serializer block
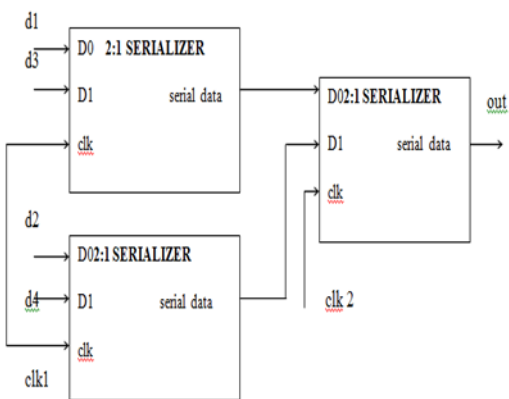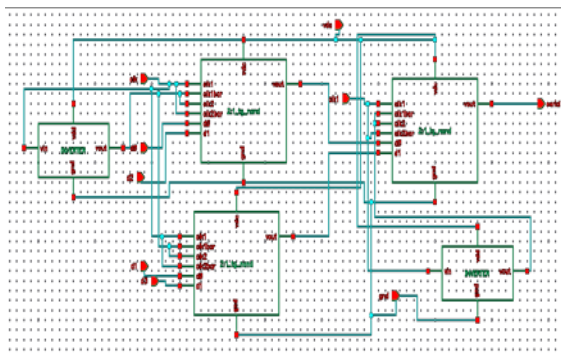

Figure 15.Generic Block of 4:1 Serializer

C. 4:1 Serializer Using DFF(Transmission gate) and MUX(NAND)

In this type of architecture we have designed the 4:1 serializer using DFF(Transmission gate) and MUX(NAND) (1101 data is serially outputed).

Figure 16.4:1 serializer using DFF(transmission gate) and MUX(pseudo)

6. PHASE LOCKED LOOP DESIGN

The PLL is used to regenerate a replica of an input frequency. It contains a Phase Comparator and a Voltage Controlled Oscillator(VCO) connected through a Low pass Filter(LPF).
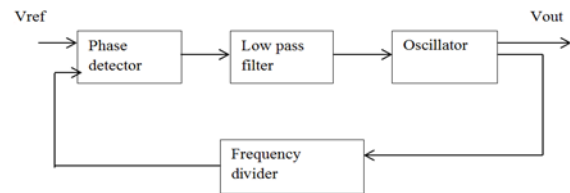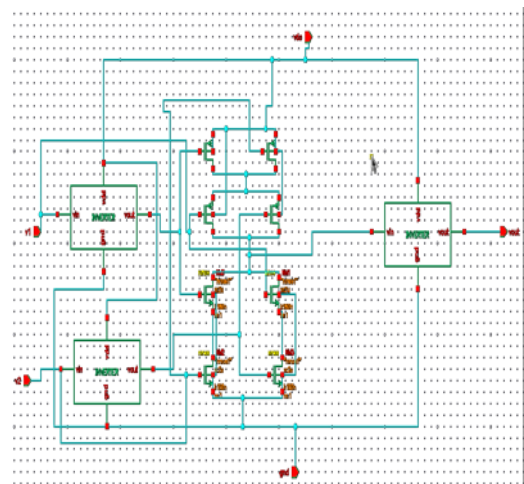

Figure 17 .Block Diagramof PLL

This forms a feedback system. The output of the VCO is compared to a reference frequency.whwnever the output frequency reaches the reference frequency the PLL is said to be in the lock condition. The block diagram of PLL is shown in Figure 5.1.
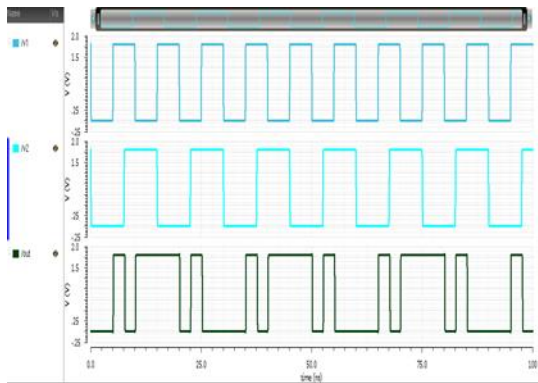
A.PhaseDetector(PD)

Figure 18.Phase Detector

The Phase Detector circuits, acts as a comparator circuit, which compares the frequency of the input signal with the VCO output frequency and produces a error voltage(DC)that is proportional to the phase difference between the two signals.
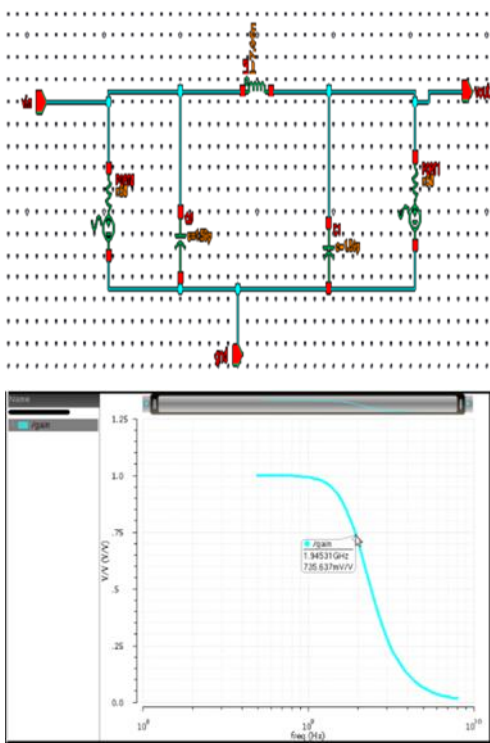
B.Low Pass Filter (LPF)

Figure 19.Low Pass Filter
Zo=50 ,fo=100MHz

L=1.51mH

C=53pF

A low-pass filter is a filter that passes signals with a frequency lower than a certain cutoff frequency and attenuates signals with frequencies higher than the cutoff frequency.The

proposed PLL used for transmitter applications, which requires a frequency of 100MHz.
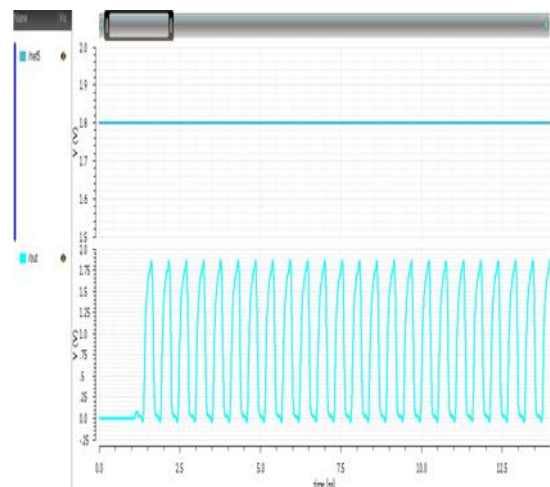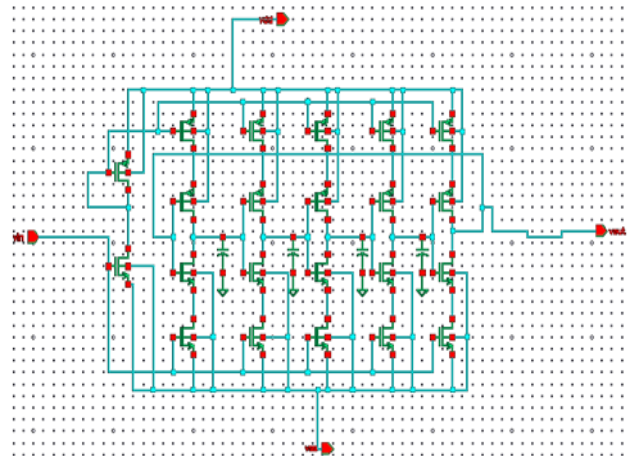
C. Voltage Controlled Oscillator (VCO)

Figure 20.VCO

An oscillator is a circuit which produces a periodic output without need of any input. Here the number of inverter stages is fixed with 5.The simplified view of a single stage current starved oscillator is shown in the Figure 20.Transistors M2 and M3 operate like an inverter while M1 and M4 operate as current sources. The current sources, Ml and M4 transistors, limit the current available to the transistor M2 and M3; in other words, the inverter is starved for current. The desired center frequency of the proposed design is 100 MHz with a supply of 1.8V[13].

D.Frequency Divider

The divider is used to scaling down the VCO frequency so that the system can operate at a frequency more than that of the reference signal.Thus the VCO has to be designed such that the output of VCO will be N times the reference frequency[14].
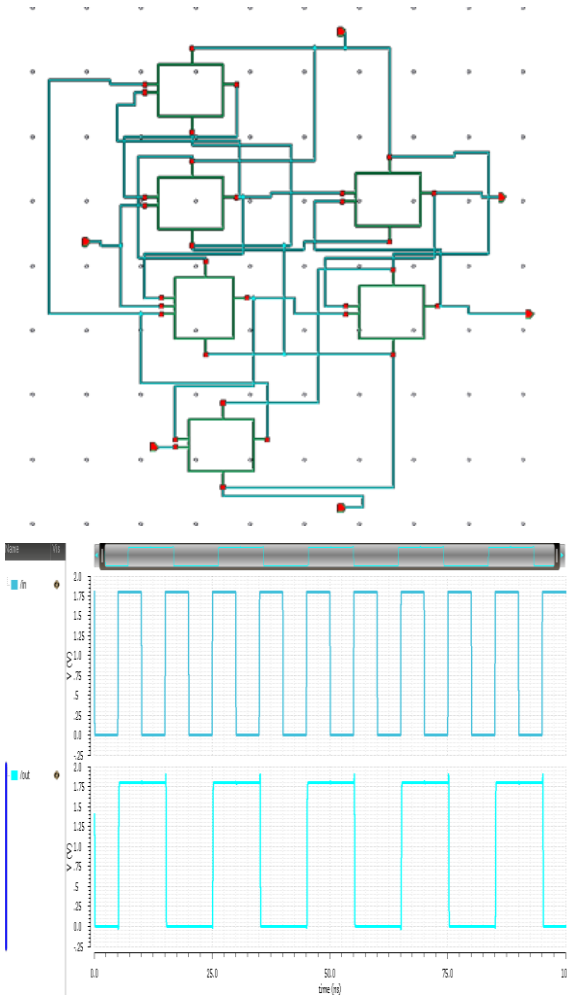
Figure 21.Frequency Divider

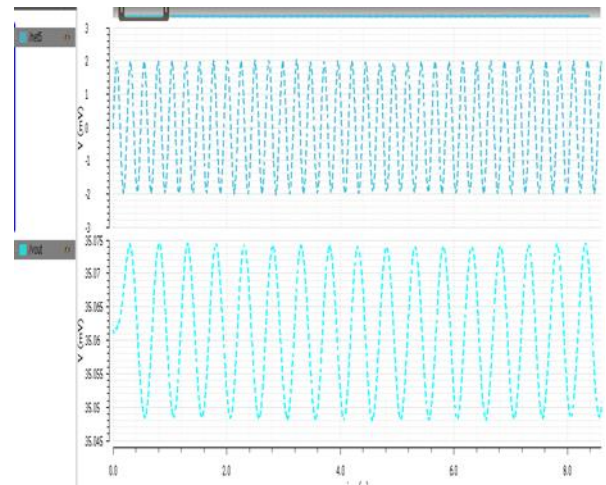The overall PLL circuit is shown below which consist of phase detector,low pass filter,vco and frequency divider.
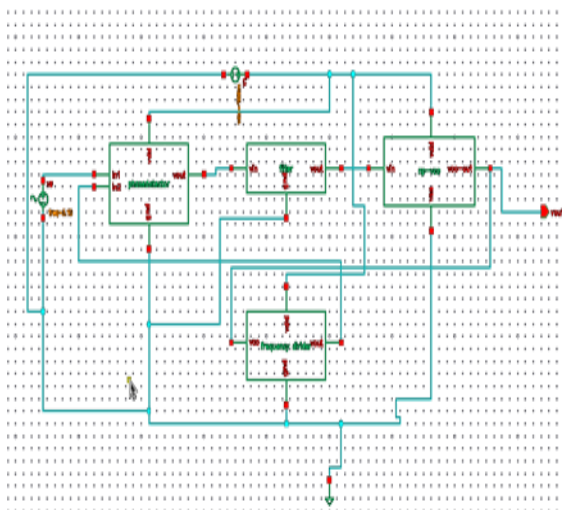
Figure 22.Phase Locked Loop

7. PLL AS CLOCK FOR SERIALIZER

A.4:1 Serializer with PLL as clock (i/p data-1011)
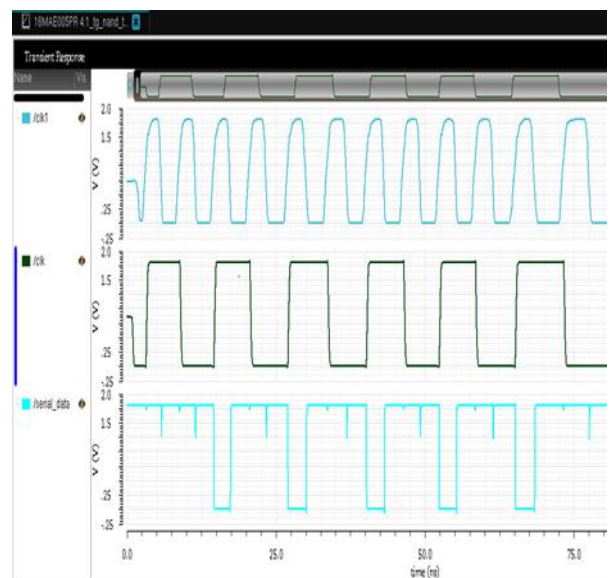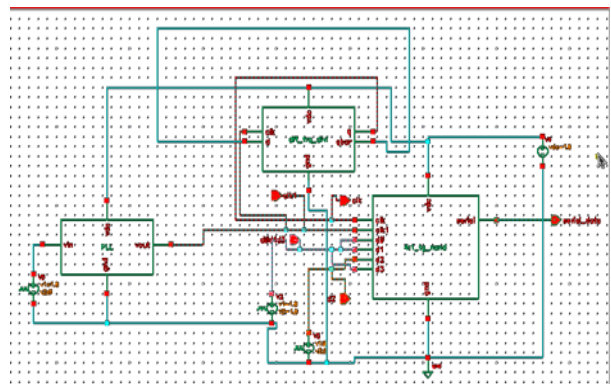
Figure 23 4:1Serializer with PLL for clock

B.4:1 Serializer with LC Filter

Our serilaized data has many high frequency components it will results big problem while receiver receving this data. So we need to remove this high frequency components. For this here LC filter is used since it results in less power and good filtering action(inputdata-1011).
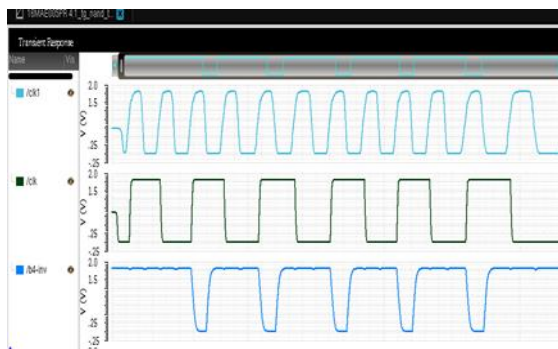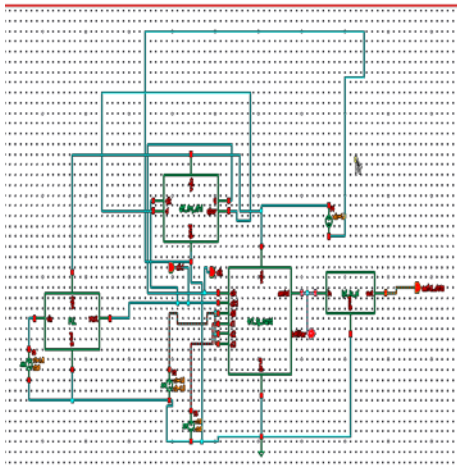
Figure 24 4:1Serializer with LC filter

C 8:1Serializer with PLL(i/p data 11011101)

Figure 25: 8:1 Serializer generic block

Figure 268:1 Serializer with PLL

D. 8:1 Serializer with Filter

Figure 278:1 Serializer with filter

8. RESULTS AND DISCUSSION

4:1 Serializer which result in low power and delay and phase locked loop is designed using the Cadence Tool Virtuoso environment and synthesized with CMOS 180nm technology standard cell library.

Table 1.Power and Delay Estimate of various Mux Design

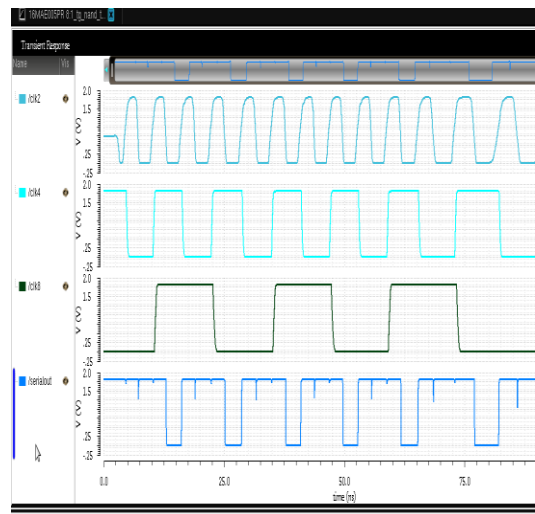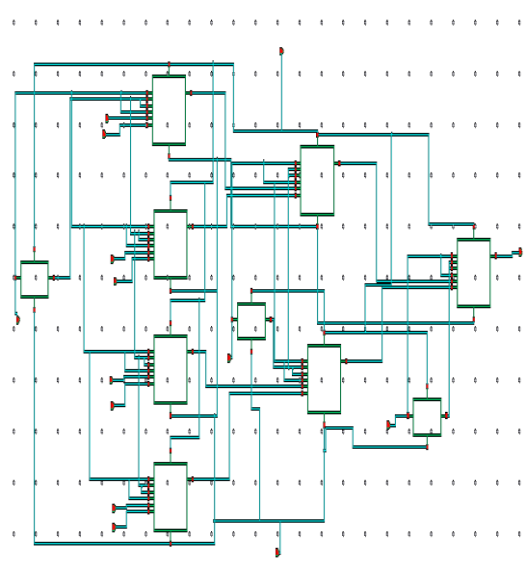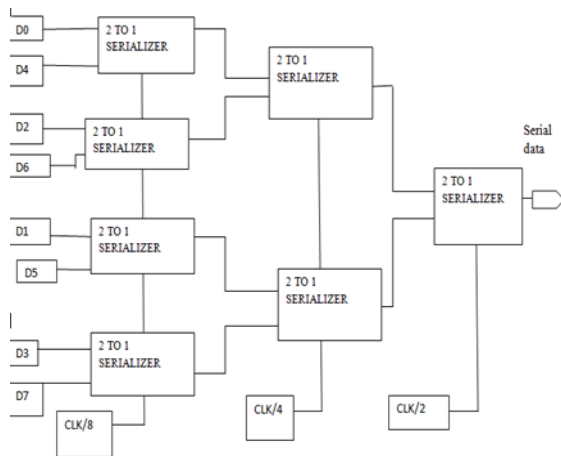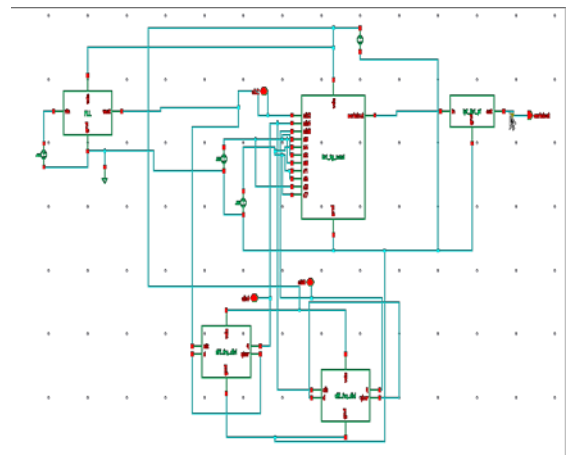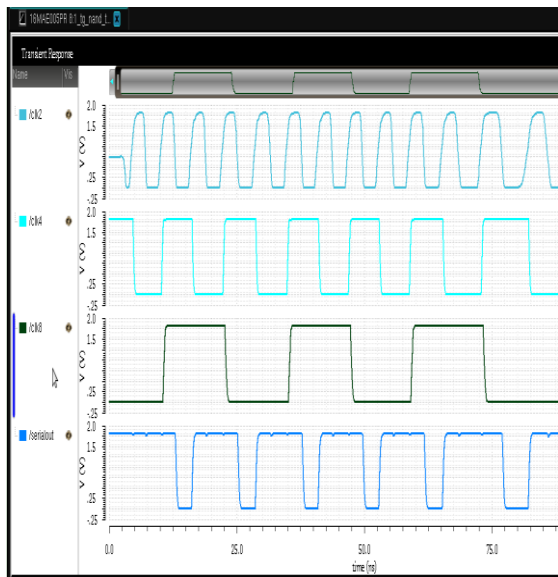| DESIGN STYLE	POWER (W)	DELAY (s)
NAND	451.0e-3	17.13e-9
Transmission gate	1.390	20.73e-9
Pass transistor	483.6e-3	17.35e-9
Inverter logic	460.7e-3	17.16e-9
Pseudo	444.5e-3	17.11e-9

It is seen from the table 1 that MUX design by pseudo logic after that NAND logicresults in low power and delay.

Table 2.Power and DelayEstimateof various D Flip Flop Design

DESIGN STYLE	POWER(W)	DELAY(s)
NAND	919.2e-3	150.7e-12
TSPC	908.6e-3	162.0e-12
Transmission gate	903.3e-3	115.3e-12
Transistor logic	906.4e-3	75.61e-9
Tristate inverter	920.2e-3	148.5e-12

It is seen from the table 2 that D FF design with transmission gate results in less power and delay.

Table 3.Power estimate of various serializer design

DATA	DFF(TG)& MUX (pseudo) Power (W)	DETFF Power (W)	DFF (TG)& MUX (NAND) Power (W)
1011	1.431	1.345	1.255
1000	692.1e-3	458.2e-3	359.2e-3
0101	1.062	899.3e-3	899.3e-3
0110	1.060	983.4e-3	810.7e-3
1001	1.062	801.5e-3	808.3e-3
1101	1.431	1.254	1.166

4:1 serilaizer is designed using transmission gate based DFF and with pseudo multiplexer ,its power is higher. Eventhoughpseudo multiplexer power is less when compared to NANDmultiplexer ,while designing 4:1 serializer its delay get increased since it consist of single pmos it should be large enough to drive the whole circuit so power get increased then 4:1 serializer designed with Transmission gate based DFF and NAND MUX results in low power when compared to the other design style.

Table 4 :The power estimate of the blocks in phase locked loop

Design units	Power(W)
PD	872.4e-3

LPF	301.3e-3
CSVCO	827.2e-3
FD	909.3e-3
PLL	25.92e-3

Table 5 : The power estimate of 4:1 serializer with filter

Input	LC(PI) power (W)
1101	1.374
1011	1.329
1010	946.6e-3
1110	1.404

Table 6 :The power estimate of 8:1 serializer with filter

Input Data	Power (W)
11011001	1.032
10110010	1.039
11011011	1.400
11011101	1.393

9. CONCLUSION

A CMOS design of 8:1 serializer based on various design style is presented. Since serialization is the basic operation need to be taken place in the place of data transmission on a chip or between the other chips. Experimental results confirm that the performance of the proposed serializer using transmission gate flip flop and MUX designed by NAND has significant reduction in terms of delay,area,power compared to the other design and also phase locked loop of about 100 MHz is designed which is used to clock the serializer.

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